A FLIP-CHIP HIGH EFFICIENCY X-BAND HPA

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Abstract

We have developed a broad band, high efficiency, X-band MMIC HPA implemented with our flip-chip technology. The amplifier utilizes PHEMT devices to achieve better than 35% PAE (40% peak) with an associated five watts of output power. The flip-chip technology reduces cost while at the same time increases performance. To our knowledge, this is the first reported flip-chip HPA that uses PHEMT devices.

Introduction

Flip-chips are a promising technology for airborne active array T/R modules. The reasons are simple: lower cost, higher yield, and improved performance. Applying this technology to high power amplifiers is a logical progression -- the improved thermal properties of a flip-chip increase output power, gain, efficiency, and reliability. Because the HPA is one of the most critical components in terms of module performance and production cost, any improvements in the HPA has a marked effect on module performance. This paper discusses the design of the first flipped PHEMT HPA.

Material Structure and Device Fabrication

The device structure and MMIC fabrication was based on a 0.25um gate, double recess, double-side-doped PHEMT MMIC process reported earlier [1]. The PHEMT structure is shown in Figure 1.

MMIC fabrication involves implant isolation, ohmic contact formation, channel recess, gate formation, SiN passivation, interconnect formation, capacitor nitride deposition, and airbridge plating. At this point the face-up and flip-chip fabrication processes diverge. A face-up wafer would proceed through thinning, via etch, and backside plating. A flip-chip wafer requires no backside processing. Instead, it proceeds directly to bump formation. Bump formation is accomplished by a dry film lamination process. The bumps are composed of silver and are used for IO interconnection or thermal shunts. The IO bumps are approximately .004" high by .006" in diameter (Figure 2). The thermal bumps are grown directly on the source pads of the FETs and are also .004" high.

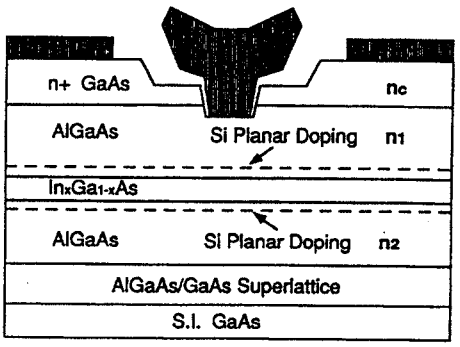

Figure 1. Cross Section of PHEMT

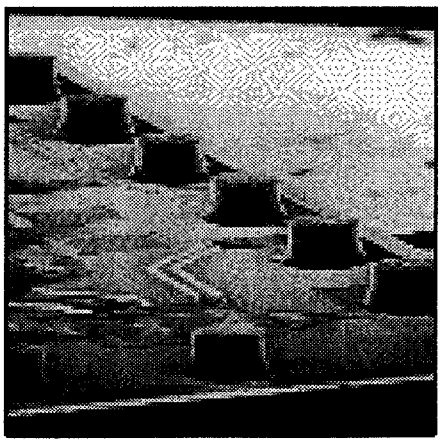

Figure 2. SEM of IO Bumps

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Flip-Chip Characteristics

Perhaps the greatest advantage of the flip-chip technology, when applied to high power amplifiers, is the low thermal resistance of an attached chip. For a conventionally mounted HPA, the heat generated in the gate region of the FET must travel though the .004" GaAs substrate which has a high thermal resistance. In the flipped case, the heat only has to travel from the gate region to a source pad where it is conducted away by the thermal bump (Figure 3). Simulated and measured data indicate that the thermal resistance of the flipped configuration is only 60% of the thermal resistance of the face-up configuration [2].

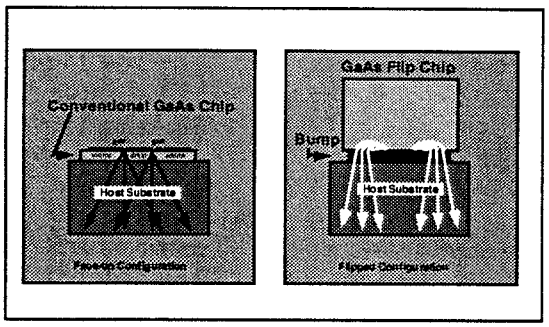

Figure 3. Face-Up vs. Flip-Chip Heat Flow

The IO bump interconnects provide several of their own advantages: the assembly cost is reduced because die attach and wirebond are now accomplished simultaneously; the solder reflow process provides self-alignment of the chip to the carrier/substrate; the interconnect has an excellent (low inductance), repeatable RF performance. Another important attribute is that the die attach process is very high yield. A yield of 99% was measured for MMICs with IO bumps only [3]. A cost model was used to project the savings this has on a T/R module build. As shown in Table 1, the yield increases by 40% and the cost is reduced by 40%.

Face-Up				Flip-Chip			
Process Step	Yield	Cost	Avail. Sites	Process Step	Yield	Cost	Avail. Sites
Start			489	Start			424
Frontside	80%	$3,000.00	391	Frontside	80%	$3,000.00	339
Backside	90%	$1,200.00	352	Bump	95%	$ 400.00	322
Wafer Test	75%	$ 360.00	264	Wafer Test	95%	$ 380.00	306
Module Assy	95%	$1,320.00	251	Module Assy	99%	$ 615.00	303
Total	51%	$5,880.00	251		71%	$4,395.00	303
Chip Cost		$ 23.44				$ 14.50	

Table 1. Cost Model Showing Advantages of Flip-Chip Technology

Design Approach

When we were assigned the task of designing a flipped PHEMT HPA an immediate problem arose - we had no recent device data for the flipped, power PHEMTs. We decided to design two amplifiers, one using recent face-up data and the other using flipped data from an earlier wafer lot. We suspected that the older flipped data would be inaccurate because the PHEMT process had undergone enhancements to optimize producibility and yield. The face-up data, on the other hand, was up to date but did not exactly represent the structure of the FET to be used in the flipped amplifier. Specifically, there are patented prematching structures that are an integral part of the device that are implemented with microstrip transmission lines. These lines had to be transformed to CPW technology before they could be used in the flip-chip design. The device topology chosen was based on the face-up version of the HPA [4].

Because PHEMT devices have such high gain, stability is a primary concern. The prematch structures were added to the FETs to reduce the low-frequency gain while at the same time increasing the input impedance. Additionally, generous amounts of bypassing and resistive loading of the bias ports helped ensure even mode stability. Odd mode stability must also be considered when designing amplifiers with parallel devices [5,6]. Ohtomo's method, which is based on control systems theory, was used to analyze the odd-mode stability problem [7]. Another stability concern is sub-harmonic oscillation due to mixing in the FET under nonlinear operation [8]. Finally, care was taken when connecting the bias ports of the stages together so as not to cause a low frequency oscillation between the stages. An efficient method used to check for bias loop oscillations is based on [9] with some modifications to ease implementation in the circuit simulator environment [10].

Fundamental to any power amplifier design is the choice of load impedance. We based ours on load-pull data from face-up devices which indicated a required load impedance of 40Ω and -0.4pF for a 1mm power cell. The output matching network is capable of providing this optimum impedance over a sizable bandwidth. In fact, current designs show promising simulated performance over an octave of frequency. The interstage matching network has the difficult task of transforming the very low input impedance of the second stage into a good power match for the first stage. The input matching network is then responsible for flattening the gain and providing a good input match. The input matching network requirements are best met with the use of lossy matching techniques [11]. Figure 4 shows a photograph of the amplifier that was based on the face-up data.

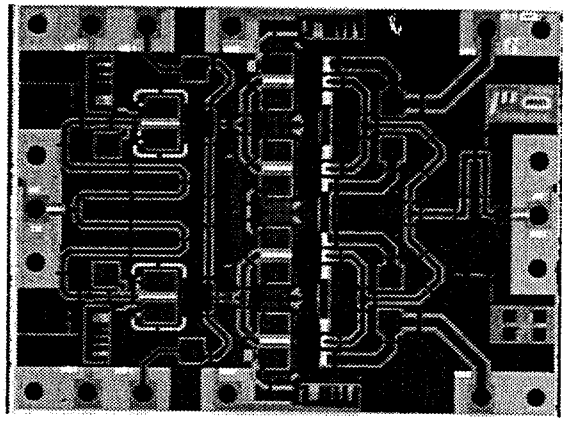

Figure 4. Photograph of Amplifier Based on Face-Up Data.

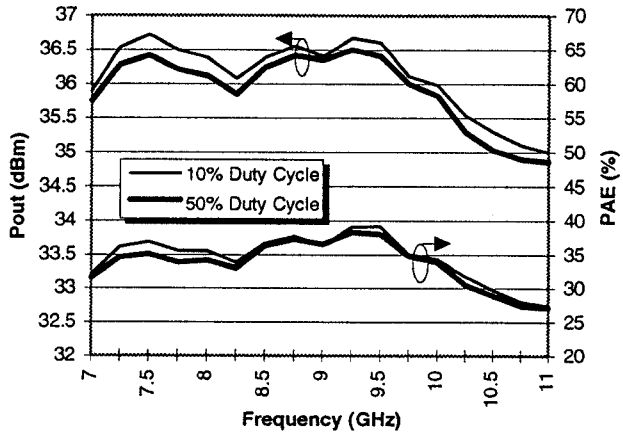

Figure 5. Mounted HPA, Pin=19dBm

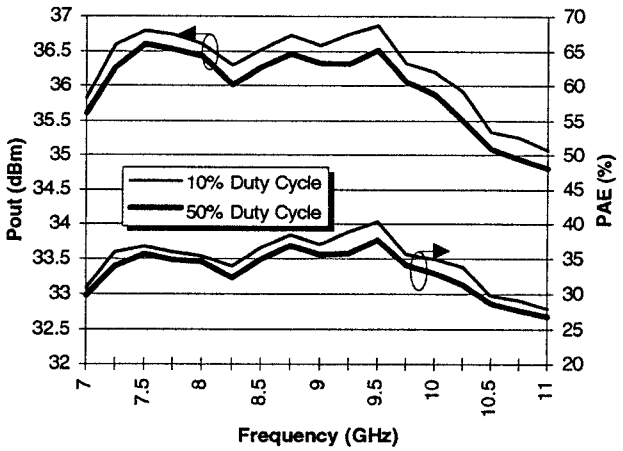

Figure 6. Unmounted HPA, Pin=19dBm

Measured Performance

Two wafer lots were fabricated. One lot was held at gate while the other lot was completely fabricated and characterized. Matching networks were then updated based on measurements of the flipped devices and the masks for the revised matching network patterns were ordered. The new masks were then used to finish the lot on hold. This procedure effectively allows us to complete two full design iterations in less than one and one-half fabrication cycle times.

Not surprisingly, the amplifier based on the recent face-up data performed better than the amplifier based on the older flipped data. We decided not to make any changes to the amplifier based on the face-up data for the half cycle update. We did, however, completely redesign the other amplifier.

Figure 5 shows the output power and power added efficiency for the updated HPA mounted to an AlN substrate. Figure 6 shows the same measurements for an unmounted version of the HPA. The measurements were performed at two duty cycles: 10% and 50% with corresponding on times of 10 μS and 50 μS. The graphs show that the performance of the mounted HPA is not as sensitive to the increased duty cycle as the unmounted HPA. Interestingly, the 10% duty cycle performance for the mounted and unmounted amplifiers is nearly identical. The reason is that there is only about 0.3 watts of power being dissipated in each device. The true benefits of decreased thermal resistance will only be seen at higher duty cycles and power levels. Currently, HPA's with much higher output powers are being designed and will benefit from these improvements.

The amplifier proved to be stable in the probe station environment, which is generally more difficult than stabilizing a fully fixtured amplifier.

Conclusion

We have developed the first flip-chip MMIC HPA utilizing a PHEMT process. The amplifier has excellent output power and efficiency over a large bandwidth. A flip-chip driver amplifier has also been developed for use with this HPA. The driver amplifier has 30 dB gain and 30% PAE over the same bandwidth as the HPA. This pair of chips makes a high performance, low cost transmit chain for airborne, active array radar applications.

References

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